REMARKS

The Final Office Action mailed on June 3, 2003, has been received and reviewed.

Claims 1-87 are currently pending in the above-referenced application. Of these, claims 18-87 have been withdrawn from consideration. Claims 1-17 again stand rejected.

While the Office has stated that the previously submitted explanations of patentability are "not commensurate with the scope of the claims," the Office has overlooked the fact that all of the explanations that have been provided by applicants refer only to language which is recited in the claims.

Moreover, it has been asserted that the rejections under 35 U.S.C. § 103(a) are "in a sense necessarily a reconstruction based upon hindsight reasoning." Nonetheless, the Office has not yet provided any convincing line of reasoning as to why one of ordinary skill in the art, without the benefit hindsight provided by the disclosure of the above-referenced application, would have been motivated to make the reference combinations that have been asserted by the Office, as required by M.P.E.P. § 2142.

Reconsideration of the above-referenced application is respectfully requested.

Information Disclosure Statement

Please note that an Information Disclosure Statement was filed in the above-referenced application on April 7, 2003, but that the undersigned attorney has not yet received an initialed copy of the Form PTO/SB/08 that accompanied that Information Disclosure Statement. It is respectfully requested that the information listed in the Information Disclosure Statement of April 7, 2003, be considered and made of record in the above-referenced application and that an initialed copy of the corresponding Form PTO/SB/08 be returned to the undersigned attorney as evidence of such consideration.

Rejections Under 35 U.S.C. § 102(e)

Claims 1, 2, 8, 9, 11, 16, and 17 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,278,153 to Kikuchi et al. (hereinafter "Kikuchi").

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Kikuchi shows, in Fig. 6D, an intermediate semiconductor device structure in which a layer of resist 20 that has been disposed within and over a via-hole 23a. Kikuchi also discloses that the resist 20 can be applied by several conventional methods, including spin-coating. Col. 17, lines 63-66.

Independent claim 1 recites a method for disposing a material on a semiconductor device structure which includes "disposing . . . material on [a] surface" of a semiconductor device structure "so as to substantially fill . . . at least one recess [thereof, the] material covering [the] surface having a thickness less than a depth of said at least one recess without subsequently removing said material from said surface . . ." Additionally, independent claim 1 requires that "an upper surface of at least a portion of said material over or within said at least one recess [be] substantially planar," as recited in independent claim 1.

With respect to the requirement of independent claim 1 that "an upper surface of at least a portion of . . . material over or within . . . at least one recess [be] substantially planar," it is respectfully submitted that Kikuchi neither expressly nor inherently describes same. While resist 20 *appears* in Fig. 6D of Kikuchi to have a planar surface, Kikuchi lacks any express description that the surface of resist 20 is planar.

In response to the Office's assertion, at pages 8 and 9 of the Office Action dated December 19, 2002, that because independent claim 1 does not specify a particular type of semiconductor device (*i.e.,* the type of semiconductor device described in Kikuchi), the reasoning that spin-coating and surface tension would cause the resist 20 of Kikuchi to be nonplanar does not necessarily apply to Kikuchi and, thus, that Kikuchi expressly describes that the resist 20 within via-holes 23a is planar. This assertion is flawed. The type of semiconductor device is irrelevant, as processes that are employed and properties of the material that is used in Kikuchi have a much more significant bearing on the planarity or nonplanarity of the resist 21 than does

the fact that the device is a DRAM device, SRAM device, PROM, EEPROM, processing device, etc. As Kikuchi describes the use of a spin-coating process to introduce resist 21 into via-holes 23a, it is clear that the result of both the spin-coating process and the surface tension of the resist would be nonplanarity of the surface of resist 21 within the via-holes 23a.

Moreover, it is respectfully submitted that Kikuchi lacks any inherent description that the method described therein results in a layer of resist 20 with a planar surface. As would be readily apparent to those of ordinary skill in the art, it is clear that the conventional spin-on processes and phororesist material employed in Kikuchi would not provide a planar surface on resist 20 which is disposed within via-holes 23a. As pointed out by the "Background" section of the specification of the above-referenced application, at page 3, line 15, to page 4, line 29, the limitations in previously known spin-on methods, as well as material properties (*e.g.,* viscosity, solids content, surface tension, adherence to adjacent materials, etc.), may prevent a layer of material, such as the resist 20 disclosed by Kikuchi and illustrated in Fig. 6D, from having a substantially planar upper surface. *See, e.g.,* Van Zandt, P., Microchip Fabrication – Chapter 8, Photolithography—Preparation to Exposure, pages 176-178 and 185-187 (hereinafter "Van Zandt"). Further, Van Zandt, at page 185, evidently recognizing that a spun-on layer of photoresist will include valleys that are located over recesses in a semiconductor substrate, describes spun-on photoresist in terms of *layer* thickness (*e.g.,* 0.5 μm to 1.5 μm thick, with variations of ± 0.01 μm) rather than in terms of surface planarity. U.S. Patent 6,117,486 to Yoshihara (hereinafter "Yoshihara") provides further evidence that the surfaces of spun-on photoresist layers may not be planar. Yoshihara, col. 1, line 18, to col. 2, line 17).

As such, it is respectfully submitted that Kikuchi does not inherently describe that resist 20 is disposed on a surface of a semiconductor device structure 21 such that the resist 20 over or within a via-hole 23a thereof has an upper surface which is substantially planar.

Furthermore, it is respectfully submitted that the foregoing arguments are commensurate with the scope of the claims since they focus on the recitation in independent claim 1 that the act of "disposing" includes forming a material layer with "an upper surface . . . over or within . . . at least one recess" of a semiconductor device structure, with the upper surface "being substantially planar."

Therefore, it is respectfully submitted that Kikuchi does not anticipate each and every element of independent claim 1, as is required to maintain a rejection under 35 U.S.C. § 102(e). Thus, under 35 U.S.C. § 102(e), independent claim 1 is allowable over Kikuchi.

Claims 2, 8, 9, 11, 16, and 17 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Claim 2, which is rejected as being anticipated by Figs 6A-6E; 10A-10E; 13A-13E, is further allowable since none of these figures shows disposing a material "so as to substantially fill . . . at least one recess *without substantially covering* [a] surface of a semiconductor device structure . . ." While various figures that have been referenced, including Figs. 6E, 10D, 10E, and 13E, show structures which include recess that are substantially filled with material while the same material does not cover the surfaces of the illustrated semiconductor devices, conventional resist-application techniques are used to apply resist to the surface of a semiconductor device, and the excess resist is subsequently removed by *another, subsequent process*. For example, etchants may be used to remove excess material (col. 18, lines 3-5; col. 26, lines 19-21) or a positive photoresist may be applied, then exposed to electromagnetic radiation, from which portions of the photoresist within recesses are shielded (col. 18, lines 5-8; col. 35, lines 40-52), with exposed and developed portions of the photoresist being subsequently washed away. Thus, Kikuchi neither expressly nor inherently describes "disposing" a material on a surface of a semiconductor device structure and within recesses thereof so as to substantially fill the recesses and "without substantially covering said surface."

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 1, 2, 8, 9, 11, 16, and 17 be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

M.P.E.P. § 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference

> or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Kikuchi in View of Yoshihara

Claims 3-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kikuchi in view of Yoshihara.

It is respectfully submitted that claims 3-7 are allowable, among other reasons, as depending either directly or indirectly from claim 1, which is itself allowable.

Moreover, neither Kikuchi, Yoshihara, nor knowledge available to one ordinarily skilled in the art suggests the combination of the teachings of Kikuchi with Yoshihara to arrive at invention which is recited in claims 3-7. Kikuchi teaches that layers of resist may be spin-coated onto semiconductor substrates that include recesses. As is well known in the art, conventional spin-coating processes result in resist layers which have substantially uniform thicknesses. However, Kikuchi neither teaches nor suggests that resist layers so formed have substantially planar surfaces, at least over or within the recesses of such semiconductor substrates. Yoshihara teaches that by spinning a semiconductor wafer at high speeds ("as low as 2000 rpm"; col. 11, line 16), lowering the speed for a time, and re-increasing it to high speeds, the wafer can be coated with material in such a way that the material layer has a substantially uniform thickness. As a layer which has a substantially uniform thickness may not also have a planar surface, it is respectfully submitted that Yoshihara does not, however, suggest that the techniques described therein are useful for disposing material within recesses such that the upper surface of at least the material within or over the recesses has a substantially planar upper surface.

As neither of these references teaches or suggests that resist or any other material within recesses of a semiconductor device structure may have a planar surface, as required by independent claim 1, it is respectfully submitted that the only way one of ordinary skill in the art could have been motivated to combine the teachings of these references in such a way as to render obvious a method which includes disposing material within a recess so that the material

has a substantially planar surface would have been to improperly glean such motivation from the description of the above-referenced application.

Accordingly, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Kikuchi and Yoshihara in the manner that has been asserted.

For the above reason, the ordinarily skilled artisan would also likely consider the likelihood of success when combining Kikuchi and Yoshihara to be quite low.

Finally, the combination does not teach or suggest each and every element of claim 5. In particular, neither Kikuchi nor Yoshihara teaches or suggests initially spinning a semiconductor device structure at a rate of about 1,000 rpm, as recited in claim 5. Instead, the initial spin rate taught by Yoshihara is "as low as 2000 rpm . . .," which is more than twice as high as the initial rate recited in claim 5. Col. 11, line 16.

In view of the foregoing, it is respectfully submitted that the Office has not set forth a *prima facie* case of obviousness against any of claims 3-7. It is, therefore, respectfully submitted that, under 35 U.S.C. § 103(a), each of claims 3-7 is allowable over the combination of Kikuchi with Yoshihara.

Kikuchi in View of Lin

Claim 10 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kikuchi in view of U.S. Patent 6,046,083 to Lin et al. (hereinafter "Lin").

It is respectfully submitted that claim 10 is allowable, among other reasons, as depending from claim 1, which is allowable.

Kikuchi in View of Park

Claims 12-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kikuchi in view of U.S. Patent 6,326,282 to Park et al. (hereinafter "Park").

It is respectfully submitted that claims 12-15 are allowable, among other reasons, as depending either directly or indirectly from claim1, which is allowable.

Election of Species Requirements

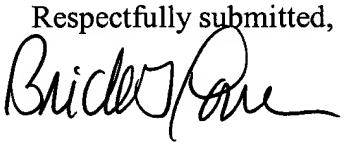
Restriction and Election of Species Requirements were made in the above-referenced application on August 12, 2001, and October 10, 2001. In responding to these requirements, it was erroneously stated that elections were being made "with traverse." As no traverse was intended and no arguments were made in support thereof, the elections that were made were made *without* traverse, as indicated in the Amendment dated May 28, 2002.

Further, it is respectfully submitted that, as independent claim 1 remains generic to all of the species of invention that have been identified by the Office, claims 18-87 should be brought back into consideration in the above-referenced application and allowed for the reasons that have been provided herein.

CONCLUSION

It is respectfully submitted that each of claims 1-87 is allowable. An early notice of the allowability of these claims and an indication that the above-referenced application has been passed for issuance are respectfully solicited. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



Brick G. Power
Registration No. 38,581
Attorney for Applicant(s)
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: July 29, 2003

Enclosure: Supplemental Information Disclosure Statement

BGP/ps:djp
Document in ProLaw